EXPEDITED PROCEDURE - EXAMINING GROUP 2823

S/N 09/745,780 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Martin Ceredig Roberts et al.	Examiner: Neal Berezny
Serial No.:	09/745,780	Group Art Unit: 2823
Filed:	December 21, 2000	Docket: 303.451US6
Title:	METHOD FOR FORMING AN INTEGRATED CIRCUIT INTERCONNECT USING A DUAL POLY PROCESS	

AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116

Box RCE
Commissioner for Patents
Washington, D.C. 20231

In response to the Final Office Action mailed June 5, 2002, please amend the application as follows:

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect cancellation of claims 46, 66 and 67 and amendment of previously pending claims 38 - 43, 45 and 48 - 52, and addition of no new claims. The specific amendments to individual claims are detailed in the following marked up set of claims.

Please cancel claims 46 and 66-67 without prejudice and amend the following claims:

38. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region [, including a field oxide region,] overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide [regions] region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the [field] oxide region; and